REMARKS

The Examiner has rejected Claims 1-2, 4-18, 20-21, 27 and 29-30 under 35 U.S.C. 112, first paragraph, as failing to comply with the written descrition requirement. In view of the Decision on Appeal mailed 03/26/2008, applicant respectfully asserts that such rejection is deemed moot.

The Examiner has rejected Claims 1, 4-18, 20, 27, and 29-30 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US Patent Number: 6,707,156) in view of Tanaka (US Patent Number: 6,100,589). Additionally, the Examiner has rejected Claims 2 and 21 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US Patent Number: 6,707,156) in view of Tanaka (US Patent Number: 6,100,589), and in further view of Applicant's Admitted Prior Art of Figures 1 and 2. Applicant respectfully disagrees with such rejections, especially in view of the amendments made hereinabove to the independent claims.

In the spirit of expediting the prosecution of the present application, applicant has amended the independent claims to distinguish applicant's claim language from the aforementioned references.

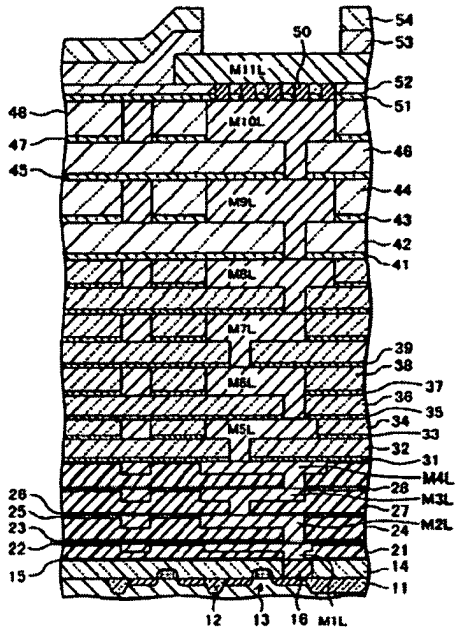
Specifically, applicant has incorporated the following subject matter into each of the independent claims to distinguish the prior art relied on by the Examiner:

"wherein the bond pad is only disposed above an outer periphery of an input/output (I/O) bus of the active circuit" (see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully notes that the Examiner has relied on item 13 of Figure 1 of the Suzuki reference to teach applicant's claimed "active circuit." However, applicant points out that Suzuki fails to specifically refer to item 13 of Figure 1 anywhere in the detailed description. Additionally, applicant notes that the Examiner has relied on an

"eleventh wiring layer M11L" (Col. 4, line 62) of Figure 1 of the Suzuki reference to teach applicant's claimed "bond pad," which is depicted in Suzuki as being located generally over item 13 in Figure 1:

FIG.1



Additionally, applicant respectfully notes that the Tanaka reference teaches that "[t]he bonding pads shown in FIG. 1 to FIG. 4 are arranged around a semiconductor chip 1000, for example, as shown in FIG. 10" and that "[a]n internal circuit 1500 is formed in the central section of the semiconductor chip 1000" (Col. 9, lines 46-52). More specifically, Figure 10 of Tanaka shows bonding pads located specifically around the internal circuit 1500 of the semiconductor chip 1000:

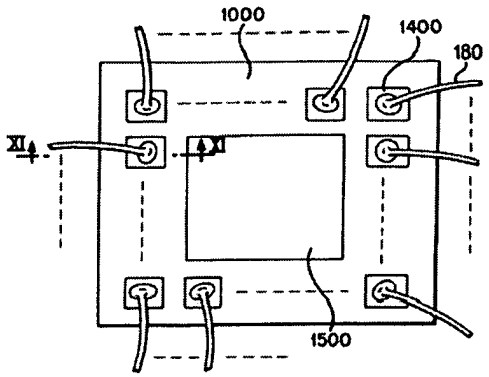


FIG. 10

However, merely disclosing a wiring layer positioned generally over an alleged active circuit, as in Suzuki, in addition to disclosing bonding pads that are arranged around a semiconductor chip, and specifically around the internal circuit of the semiconductor chip, as in Tanaka, fails to teach a technique "wherein the bond pad is only disposed above an outer periphery of an input/output (I/O) bus of the active circuit" (emphasis added), as claimed by applicant.

Additionally, applicant has amended independent claims 1 and 20 to distinguish applicant's claim language from the aforementioned references, as follows:

"wherein an interconnect metal layer of the metal layer is electrically coupled to a plurality of underlying metal layers by way of vias, the plurality of underlying metal layers disposed at least in part below the active circuit" (see this or similar, but not necessarily identidical language in the independent claims).

Applicant respectfully notes that the Tanaka reference merely discloses a "semiconductor device... that provide[s] highly reliable and high density arrangement of a connecting region for an external connecting terminal, such as a bonding pad" (Abstract – emphasis added). Additionally, the Suzuki reference discloses "[a] multilevel wiring structure" which includes "a number of semiconductor elements formed on [a] semiconductor substrate" as well as "a plurality of lower level wiring layers electrically

connected to the semiconductor elements" and "a plurality of first insulating layers electrically separating the lower level wiring layers" (Abstract – emphasis added).

However, merely disclosing a connecting region on a semiconductor device for a bonding pad, as in Tanaka, in addition to disclosing semiconductor elements that are electrically connected to lower level wiring layers, with insulating layers electrically separating the lower level wiring layers, as in Suzuki, fails to teach a technique "wherein an interconnect metal layer of the metal layer is electrically coupled to a plurality of underlying metal layers by way of vias, the plurality of underlying metal layers disposed at least in part below the active circuit" (emphasis added), as claimed by applicant. Nowhere in the above references is an "interconnect metal layer" taught which "is electrically coupled to a plurality of underlying metal layers by way of vias," where "the plurality of underlying metal layers [are] disposed at least in part below the active circuit" (emphasis added), in the context claimed.

Further, applicant has amended independent claim 21 to distinguish applicant's claim language from the aforementioned references, as follows:

"wherein the interconnect metal layer is electrically coupled to the plurality of underlying metal layers by way of vias."

Applicant again respectfully notes that merely disclosing a semiconductor device that provides a connecting region for a bonding pad, as in Tanaka, in addition to disclosing semiconductor elements that are electrically connected to lower level wiring layers, with insulating layers electrically separating the lower level wiring layers, as in Suzuki, fails to teach a technique "wherein the interconnect metal layer is electrically coupled to a plurality of underlying metal layers by way of vias" where the "plurality of vertically spaced underlying metal layers [is] disposed, at least partially, under the active circuit" (emphasis added), in the context claimed by applicant.

Additionally, applicant notes that the Applicant's Admitted Prior Art relied on by the Examiner to meet applicant's claimed "underlying metal layers" discloses that "underlying metal layers **206** are further coupled to the bond pads **106**" (Page 2, lines 5-6). However, disclosing that the underlying metal layers are coupled to the bond pads fails to disclose a technique "wherein the interconnect metal layer is electrically coupled to a plurality of underlying metal layers by way of vias" (emphasis added), as claimed by applicant. Nowhere in the above references is an "interconnect metal layer" taught which "is electrically coupled to a plurality of underlying metal layers by way of vias," where the "plurality of vertically spaced underlying metal layers [is] disposed, at least partially, under the active circuit" (see Claim 21 - emphasis added), in the context claimed.

Further, applicant has amended the independent claims to distinguish applicant's claim language from the aforementioned references, as follows:

"wherein the interconnect metal layer interconnects the bond pad with the plurality of underlying metal layers" (see this or similar, but not necessarily identidical language in the independent claims).

Applicant respectfully notes that the Tanaka reference merely discloses a "semiconductor device... that provide[s] highly reliable and high density arrangement of a connecting region for an external connecting terminal, such as a bonding pad" (Abstract – emphasis added). Additionally, the Suzuki reference discloses "[a] multilevel wiring structure" which includes "a number of semiconductor elements formed on [a] semiconductor substrate" as well as "a plurality of lower level wiring layers electrically connected to the semiconductor elements" and "a plurality of first insulating layers electrically separating the lower level wiring layers" (Abstract – emphasis added).

However, merely disclosing a semiconductor device that provides a connecting region for a bonding pad, as in Tanaka, in addition to disclosing semiconductor elements that are electrically connected to lower level wiring layers, with insulating layers electrically separating the lower level wiring layers, as in Suzuki, fails to teach that "the

interconnect metal layer interconnects the bond pad with the plurality of underlying metal layers," especially where "the interconnect metal layer is electrically coupled to a plurality of underlying metal layers by way of vias, the plurality of underlying metal layers disposed at least in part below the active circuit" (emphasis added), in the context claimed by applicant (see this or similar, but not necessarily identidical language in the independent claims).

Further still, applicant has amended the independent claims to further distinguish applicant's claim language from the aforementioned references, as follows:

"wherein the interconnect metal layer of the metal layer is meshed by including a plurality of openings, the openings defining a plurality of substantially linear first portions and a plurality of substantially linear second portions which intersect, where interconnect vias formed in rows along a length of at least the first portions provide communication between the interconnect metal layer and the bond pad" (see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully notes that the Tanaka reference merely discloses that "a bonding pad having a triple layer structure comprises... a first insulating interlayer 160 provided with a plurality of through holes" and that "conductive members 120a to 120d [are] embedded into the through holes provided in the insulating interlayer 160" (Col. 6, lines 20-25 – emphasis added) Additionally, the Tanaka reference discloses "a second insulating interlayer 150 provided with a plurality of through holes" where "conductive members 110a to 110d [are] embedded into the through holes provided in the insulating interlayer 150" (Col. 6, lines 26-29 – emphasis added).

However, merely disclosing insulating interlayers **of a bond pad** that are provided with a plurality of through holes where conductive members are embedded, , as in Tanaka, fails to disclose a technique "wherein the **interconnect metal layer** of the metal layer is meshed by including a plurality of openings, the openings defining a plurality of substantially linear first portions and a plurality of substantially linear second

portions which intersect, where interconnect vias formed in rows along a length of at least the first portions provide communication between the interconnect metal layer and the bond pad," and where the "bond pad [is] disposed, at least partially, above the metal layer" (see independent Claims 1 and 20 – emphasis added), and where "a top metal layer [is] disposed, at least partially, above the inter-metal dielectric layer, the top metal layer for serving as a bond pad" (see independent Claim 21 – emphasis added), in the context claimed by applicant.

In addition, applicant has amended the independent claims to further distinguish applicant's claim language from the aforementioned references, as follows:

"wherein the openings are adapted for facilitating an interlock between the interconnect metal layer of the metal layer and the inter-metal dielectric layer" (see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully notes that the Suzuki and Tanaka references merely disclose "a bonding pad having a triple layer structure comprises... a first insulating interlayer 160 [is] provided with a plurality of through holes" and "conductive members 120a to 120d [are] embedded into the through holes provided in the insulating interlayer 160" (Tanaka, Col. 6, lines 20-25 – emphasis added) Additionally, the references disclose "a second insulating interlayer 150 provided with a plurality of through holes" where "conductive members 110a to 110d [are] embedded into the through holes provided in the insulating interlayer 150" (Tanaka, Col. 6, lines 26-29 – emphasis added).

However, merely disclosing insulating interlayers of a bond pad that are provided with a plurality of through holes where conductive members are embedded, as in Tanaka, fails to disclose a technique "wherein the openings are adapted for facilitating an interlock between the interconnect metal layer of the metal layer and the inter-metal dielectric layer," where "the interconnect metal layer of the metal layer is meshed by including a plurality of openings" and where the "bond pad [is] disposed, at least

partially, above the metal layer" (as amended, see independent Claims 1 and 20 – emphasis added), as claimed by applicant.

Additionally, merely disclosing insulating interlayers of a bond pad that are provided with a plurality of through holes where conductive members are embedded, as in Tanaka, fails to disclose a technique "wherein the openings are adapted for facilitating an interlock between the interconnect metal layer of the metal layer and the inter-metal dielectric layer," where "the interconnect metal layer of the metal layer is meshed by including a plurality of openings" and where "a top metal layer [is] disposed, at least partially, above the inter-metal dielectric layer, the top metal layer for serving as a bond pad" (as amended, see independent Claim 21 – emphasis added).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*,947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art excerpts, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above.

Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

In this way, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP234).

Respectfully submitted,
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